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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,170	11/14/2001	Eugene P. Matter	42390P12396	7336

8791 7590 05/25/2004

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	14

DATE MAILED: 05/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,170	MATTER ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-10,12 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-12 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 31, 2004 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 10, 12, 16 and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Ingerman (USPN: 5,636,361).

Regarding claims 10, 12 and 20-21, Ingerman discloses a memory array (memory array is comprised of References 34, 42, 48 and 52 in Figure 2) having a first portion (Figure 2, Reference 34) and a second portion (Figure 2, Reference 52); a first processor (Figure 2, Reference 32); and a second processor (Figure 2, Reference 50), wherein the first portion of the memory array is directly accessible only by the first processor via a first bus (the first bus is coupled, to the first port of memory portion Reference 34, between References 32 and 34; C 6, L 45-47), and the second portion of the memory array is directly accessible only by the second

processor via a second bus (the second bus is coupled, to the second port of the memory portion Reference 52, between References 50 and 52; C 6, L 55-57).

Regarding claim 16, Ingerman discloses the memory array further comprising a third portion (Figure 2, References 42 and 48) that is different than the first portion and the second portion, wherein the third portion of the memory array is accessible by both the first processor and the second processor (C 7, L 17-26).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama et al. (USPN: 5,140,681) in view of Cherabuddi (PGPUB: US 2002/0184445).

Uchiyama discloses an apparatus comprising a memory array (Figure 5; Figure 2, Reference 5) having a first portion (Figure 5, Reference 61) and a second portion (Figure 5, Reference 62), the first portion of the memory array being different than the second portion of the memory array, wherein the memory array is adapted such that the first portion of the memory array is accessible only by a first processor (C 5, L 28-31) and the second portion of the memory array is accessible only by a second processor (C 5, L 30-31), wherein the memory array further comprises a third portion that is different than the first portion and the second portion (Figure 5, References 60 and

63), the third portion of the memory array accessible by both the first processor and the second processor (C 5, L 26-28). Uchiyama does not disclose dynamically altering a size of the first and second portion of the memory array depending on an operational load of the first and second processor. However, Cherabuddi discloses dynamically altering a size of the first portion and the second portion of the memory array depending on an operational load (indicated by the active state of the processor) of the first and second processor (pages 2-3, section [0025] – when the system operates in state 1T, the first portion size is doubled and the second portion size is zero). This feature taught by Cherabuddi provides improved performance by providing efficient memory usage based on the operating conditions of the system. Hence, it would have been obvious to one of ordinary skill in the art to use Cherabuddi's teachings with the system taught by Uchiyama for the desirable purpose of improved performance and efficiency.

6. Claims 1, 3-4 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cherabuddi (PGPUB: US 2002/0184445) in view of Uchiyama et al. (USPN: 5,140,681). Regarding claims 1, 3-4, 6 and 9, Cherabuddi discloses an apparatus comprising a memory array (Figure 2, Reference 23) having a first portion (Figure 2, Reference 23a) and a second portion (Figure 2, Reference 23b), the first portion of the memory array being different than the second portion of the memory array (page 2; section [0019]; lines 6-9), wherein the memory array is adapted such that the first portion of the memory array is accessible only by a first processor (Figure 2, Reference 21a) and the second portion of the memory array is accessible only by a second processor (Figure 2, Reference 21b) (page 2; section [0023], lines 11-19). Cherabuddi discloses dynamically altering a size of the first portion and the second portion of the memory array depending on an operational load (indicated by the active state of the processor) of the first

and second processor (pages 2-3, section [0025] – when the system operates in state 1T, the first portion size is doubled and the second portion size is zero). Cherabuddi does not disclose a third portion of memory different than the first and second portion of memory, wherein the third portion of the memory array is accessible by the first processor and the second processor. Uchiyama teaches a memory array comprising a third portion that is different than the first portion and the second portion (Figure 5, References 60 and 63), the third portion of the memory array accessible by both the first processor and the second processor (C 5, L 26-28). This feature taught by Uchiyama allows data sharing in the shared partition and allows non-data sharing in the private partition, which provides flexibility. In Cherabuddi, the partitions are dedicated and do not allow for data sharing. Hence, it would have been obvious to one of ordinary skill in the art to use Uchiyama's teachings with the system taught by Cherabuddi for the desirable purpose of flexibility and improved performance.

Regarding claims 7-8, Cherabuddi discloses the first processor accessing the first portion of the memory array substantially simultaneously as the second processor access the second portion of the memory array (pages 3-4, section [0034]; - the first and second processor are granted exclusive access simultaneously to the first and second amount of memory and thus the first processor may read to the first portion of memory simultaneous with the second processor writing to the second portion of memory).

7. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ingerman (USPN: 5,636,361) in view of Cherabuddi (PGPUB: US 2002/0184445).

Regarding claims 18-19, Ingerman discloses dynamically altering a size of the third portion of the memory array depending on the operational load of the system (C 7, L 60-67). However, Ingerman does not disclose altering the first portion and the second portion of the memory array depending on an operational load of the first processor or the second processor. Cherabuddi discloses dynamically altering a size of the first portion and the second portion of the memory depending on an operational load (indicated by active state of the processor) of the first processor or the second processor (pages 2-3; section [0025] – when the system operates in state 1T, the first portion size is doubled and the second portion size is zero). This feature taught by Cherabuddi provides efficiency by allocating the memory portions to accommodate the workload of the system, which improves the performance of the system. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to also dynamically alter the first and second memory portions of Ingerman's memory array for the desirable purpose of efficiency.

Response to Arguments

8. Applicant's arguments filed have been fully considered but they are not persuasive. Regarding Applicant's arguments regarding claims 1, 3-4 and 6-9, the above rejection is a 35 U.S.C. 103 rejection, which implies that a single reference does not teach all of the claimed limitations. Accordingly a secondary reference is provided which teaches that which is not taught in the primary reference. In this case, Cherabuddi, in paragraph 3, is relied upon for teaching dynamically altering a first and second memory portion depending on an operational load of a first and second processor and not for teaching exclusive access to the memory

portions, which is already taught by the primary reference Uchiyama. Hence, the combined teachings of Uchiyama and Cherabuddi disclose the claimed invention.

Regarding Applicant's arguments with respect to the teachings of Ingerman, it should be noted that claim limitations are examined given the broadest reasonable interpretation. In this instance, memory array does not explicitly mean, "not separate". Hence, a memory array may comprise more than one memory device. As such, the interpretation used in rejected the claim limitations is valid and Ingerman teaches the claimed invention.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

May 24, 2004